Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte NORIAKI KODAMA

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Appeal No. 2001-2659
Application 08/919,674

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ON BRIEF

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Before OWENS, DELMENDO and POTEATE, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-13, which are all of the claims in the application.

THE INVENTION

The appellant claims a method for making a nonvolatile semiconductor storage device comprising, on the same semiconductor base, 1) a two-layered gate electrode having a floating gate and a control gate, and 2) a MOS transistor, for use in a peripheral circuit, having a single gate electrode.

Claim 1 is illustrative:

1. A method for manufacturing a nonvolatile semiconductor storage device comprising the steps of:

forming an element separating oxide layer onto a semiconductor base for defining a first region for forming a nonvolatile memory cell and a second region for forming an MOS transistor for use in a peripheral circuit;

forming a first gate insulating layer on said first and second regions of a surface of said semiconductor base;

forming a first polysilicon layer over the entire surface of said semiconductor base, and then patterning said first polysilicon layer in a manner such that said first polysilicon layer is left covering only said first gate insulating layer of said first region;

sequentially forming a second gate insulating layer having three insulating layers and a second polysilicon layer over the entire surface of said first region and said second region;

sequentially removing said second polysilicon layer, said second gate insulating layer and said first gate insulating layer, respectively, in said second region;

forming a third gate oxide layer over a surface of said semiconductor base corresponding to said second region by means of thermal oxidation;

coating a third polysilicon layer over the entire surface of said first region and said second region, and patterning said third polysilicon layer to form a gate electrode over said second region; and

patterning said second polysilicon layer, said second gate insulating layer, and said first polysilicon layer to form a gate electrode in said first region wherein a control gate is formed by patterning said second polysilicon layer, said second gate insulating layer and said first polysilicon layer, and a floating gate is formed by patterning said first polysilicon layer.

THE REFERENCE

Kume et al. (Kume) 5,188,976 Feb. 23, 1993

THE REJECTION

Claims 1-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kume.

OPINION

We reverse the aforementioned rejection and remand the application to the examiner. We need to address only the independent claims, i.e., claims 1, 2, 10 and 12.

Claims 1 and 2

"Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference." *Corning Glass Works v. Sumitomo Electric*, 868 F.2d 1251, 1255-56, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).

Both of claims 1 and 2 require the step of "forming a first polysilicon layer over the entire surface of said semiconductor base, and then patterning said first polysilicon layer in a manner such that said first polysilicon layer is left covering only said first gate insulating layer of said first region". Claims 1 and 2 do not require that the steps are carried out in the recited order. However, the forming and patterning in the

above-recited step must be carried out sequentially since this is a single step.

Kume forms a first polysilicon layer (5) over the entire surface of a semiconductor base, and then patterns the first polysilicon layer such that it covers a gate insulating layer (3) of both first and second regions (i.e., the first area and second area in figure 1A) (col. 5, lines 45-53).[1,2] Thus, in this step Kume does not pattern the first polysilicon layer in a manner such that it is left covering only the first gate insulating

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[1] The appellant's argument (brief, pages 10-11) that Kume's gate oxide layer (3) is not a gate insulating layer is without merit. As was well known in the semiconductor art, a gate oxide layer is a gate insulating layer. *See, e.g.*, S.M. Sze, *Physics of Semiconductor Devices* 453 (John Wiley & Sons, 2nd ed. 1981); Sumner N. Levine, *Principles of Solid-State Microelectronics* 178 (Holt, Rinehart & Winston, 1963). A copy of the relevant page of each of these references is provided to the appellant with this decision.

[2] The appellant argues that Kume's gate oxide layer 3 is not equivalent to the appellant's first gate insulating layer (3) because the appellant's first gate insulating layer is at least partially removed (figure 1C) whereas Kume's gate oxide layer 3 is not disclosed as being removed but, rather, is heated to form gate oxide film 8 (reply brief, page 2). This argument is not well taken because the presence of Kume's gate oxide layer 3 in the second area in figure 1C, and the absence of that gate oxide layer from the second area in figure 1D, indicates that in the etching disclosed by Kume (col. 6, lines 17-24), gate oxide layer 3 is removed. Kume teaches that gate oxide layer 8 subsequently is formed by thermal oxidation (col. 6, lines 25-29).

layer of the first region as required by the appellant's claims 1 and 2. The first polysilicon layer in the second region is not removed in this step because the first polysilicon layer is used as a buffer layer for preventing the semiconductor substrate surface from being contaminated or damaged when a subsequently-applied interlayer insulating film (6) is etched from the second region (col. 6, lines 1-5). Kume's first polysilicon layer is not removed until after carrying out the next step in the appellant's method, i.e., "sequentially forming a second gate insulating layer having three insulating layers and a second polysilicon layer over the entire surface of said first and said second region".[3] Thus, Kume's interlayer insulating film (6) and second polycrystalline layer (7) are formed in the second region on the first polysilicon layer (5) (figure 1B), whereas the appellant's second gate insulating layer (8) and second polysilicon layer (9) are formed in the second region on the first gate insulating layer (3) (figure 1B).

[3] Kume forms on the first polysilicon layer an interlayer insulating film (6) and then a second polycrystalline layer (7) (col. 5, lines 59-64; figure 1B), and then removes the second polycrystalline layer, the interlayer insulating film and the first polysilicon layer from the second region (col. 5, lines 65-68; figure 1C).

The examiner argues that "[t]he 1st polysilicon layer is removed from the 2nd region, and the 2nd polysilicon layer is removed from the 2nd region (see Figs. [sic] 1C)" (answer, page 3). The examiner, however, does not point out any disclosure in Kume wherein the first polysilicon layer is removed from the second region before the intermediate insulating film and second polycrystalline layer are formed in that region.

The examiner, therefore, has not carried the burden of establishing a *prima facie* case of anticipation of the method claimed in the appellant's independent claims 1 and 2. Accordingly, we reverse the rejection of these claims and dependent claims 3-9.

Claim 10

Kume discloses a method for manufacturing a nonvolatile semiconductor storage device (col. 1, lines 8-9), comprising the steps of:

1) selectively oxidizing a surface of a silicon semiconductor substrate (11) (col. 7, lines 46-48) according to the LOCOS method (col. 8, lines 65-67) so as to form an element separating oxide layer (14) which defines an elemental area (figure 7, memory transistor area) and a peripheral circuit transistor region (figure 7, peripheral circuit MOS transistor

area);

2) forming a first gate insulating layer (16) on the surface of the elemental area (figure 7; col. 9, lines 61-63);

3) depositing a first polysilicon layer (17), for forming a floating gate, over the entire surface of the silicon base (figure 7; col. 9, line 63 - col. 10, line 4);

4) forming a second gate insulating layer (18, 19, 20) having an ONO structure consisting of a first silicon oxide layer (18) formed by thermal oxidation, a silicon nitride layer (19) formed by chemical vapor deposition, and a second silicon oxide layer (20) formed by thermal oxidation (figure 7; col. 10, lines 7-16);

5) forming a second polysilicon layer (21) onto the second gate insulating layer (18, 19, 20) (figure 7; col. 10, lines 17-21);

6) selectively removing the second polysilicon layer (21) in the peripheral circuit transistor region and in the second gate insulating layer (18, 19, 20) by means of an etching process, and patterning the first polysilicon layer (17) such that it is selectively left covering only the elemental area,[4] (figure 9;

[4] The appellant's claims do not require that the steps are carried out in the recited sequence.

col. 10, lines 30-49);

7) forming a gate oxide layer (27) in the peripheral circuit transistor region and forming a silicon oxide layer (27') onto the second polysilicon layer (21) (figure 9; col. 10, lines 51-58);

8) depositing a third polysilicon layer (lower layer of tungsten polycide layer 28) onto the entire surface so as to form a gate electrode of a peripheral transistor (figure 9; col. 10, line 59 - col. 11, line 3);

9) patterning the third polysilicon layer (28) so as to form a gate electrode comprising the third polysilicon layer (28) in the peripheral circuit transistor region while using the silicon oxide layer (27') as a protective layer for the second polysilicon layer (21) (figure 11; col. 11, lines 3-15);[5] and

10) patterning the second polysilicon layer (21), the second gate insulating layer (18, 19, 20), and the first polysilicon layer (17) so as to respectively form a control gate from the second polysilicon layer (21), and a floating gate from the first polysilicon layer (17) in the elemental area (figure 11; col. 11,

[5] Thus, the appellant's argument (reply brief, page 3) that Kume does not pattern the third polysilicon layer while using the silicon oxide layer (27') as a protective layer for the second polysilicon layer is incorrect.

lines 19-33).

Thus, the method claimed in the appellant's claim 10 differs from Kume's method only in that Kume's oxide layers (18) and (20) of the second gate insulating layer (18, 19, 20) are formed by thermal oxidation rather than by chemical vapor deposition. Because of this difference, however, Kume does not anticipate the claimed method. Consequently, we reverse the rejection of claim 10 and claim 11 which depends therefrom.

Claim 12

The first 8 steps of claim 12 are addressed in steps 1-7 of the above discussion of claim 10. Kume also discloses the steps of:

8) depositing a third polysilicon layer (28) onto the entire surface so as to form a gate electrode of a peripheral circuit transistor (figure 12; col. 11, lines 66-68);

9) removing, by means of an etching process, the third polysilicon layer (28) of the memory cell array region and the silicon oxide layer (27') formed on the surface of the second polysilicon layer (21) (figure 12; col. 11, lines 7-15; col. 12, lines 1-3);

10) depositing a WSi layer (40) over the entire surface (figure 12; col. 12, lines 4-7); and

11) patterning the WSi layer (40) along with the third polysilicon layer (28), the second polysilicon layer (21), the second gate insulating layer (18, 19, 20) and the first polysilicon layer (17), so as to form, in the peripheral circuit transistor region, a gate electrode from the WSi layer (40) and the third polysilicon layer (28), and to form, in the memory array region, a control gate from the WSi layer (40) and the second polysilicon layer (21), and a floating gate from the first polysilicon layer (17) (figure 13; col. 12, lines 13-27).

As discussed above regarding claim 10, Kume does not disclose forming the oxide layers (18 and 20) of the second gate insulating layer (18, 19, 20) by chemical vapor deposition as required by claim 12.[6] Accordingly, we reverse the rejection of this claim and claim 13 which depends therefrom.

REMAND

We remand the application to the examiner for the examiner to reopen prosecution and for the examiner and the appellant to address on the record whether Kume, alone or in combination with additional prior art, would have fairly suggested, to one of ordinary skill in the art, the above-discussed requirements of

[6] This is the only difference between the method claimed in the appellant's claim 12 and Kume's method.

the appellant's claims which are not disclosed by Kume.[7]

DECISION

The rejection of claims 1-13 under 35 U.S.C. § 102(b) over Kume is reversed. The application is remanded to the examiner.

REVERSED and REMANDED

TERRY J. OWENS Administrative Patent Judge	)
ROMULO H. DELMENDO Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
LINDA R. POTEATE Administrative Patent Judge	)

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[7] A supplemental answer is not authorized.

Helfgott & Karas
Empire State Building
60th Floor
New York, NY 10118-0110